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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/976,930	10/11/2001	Clifford L. Hersh	PA1950US	2048

22830 7590 05/03/2005

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EXAMINER	
SHAH, NILESH R	

ART UNIT	PAPER NUMBER
2195	

DATE MAILED: 05/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/976,930	HERSH, CLIFFORD L.	
	Examiner	Art Unit	
	Nilesh Shah	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-40 are presented for examination.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-40 are rejected under 35 U.S.C. 102(b) as being anticipated by Gostanian et al (5,781,910) (hereinafter Gostanian).

4. As per claim 1, Gostanian teaches a method for executing an operation upon a linked data method comprising structure having at least one element, steps of:

performing a first set of operation tasks in a phase, the first set of operation tasks operable to effect a first of element state transitions (col. 6 lines 6-17;col. 10 lines 30-50);

developing a second set operation tasks the second operation tasks operable effect a second set element state transitions, the second set of element state transitions being distinct from the set of element state transitions(col. 13 lines 40-65); and

performing second set of operation tasks in a second phase(col. 13 lines 40-65; col. 16 lines 53-57).

5. As per claim 2, Gostanian teaches a method wherein the first set operation tasks structure links(col. 3 lines 1-21).

6. As per claim 3, Gostanian teaches a method wherein step developing a second set of operation tasks further comprises developing pointers the data structure, the pointers being used the step of performing the second set of operation tasks in second phase(col. 13 lines 40-65; col. 16 lines 53-57).

7. As per claim 4, Gostanian teaches a method wherein operation tasks operation of the second set tasks are performed atomically (col. 6 lines 19-40).

8. As per claim 5, Gostanian teaches a method wherein the step of developing a second set of operation tasks further comprises developing the second set of operation tasks as a list (col. 9 lines 43-55).

9. As per claim 6, Gostanian teaches a method wherein the list further comprises a first in last out list (col. 14 lines 64-67;col. 19 lines 31-40; col. 14 lines 18-41).

10. As per claim 7, Gostanian teaches a method wherein the step developing a second set of operation tasks further comprises a step check for the operation performing a conflicts check for the operation (col. 14 lines 20-42).

11. As per claim 8, Gostanian teaches a method wherein the first set of element state transitions further comprises:

a valid state to a pending delete state transition(col. 1 lines 40-50;col. 15 lines 10-25);

a pre-associated state to a pending insert state transition(col. 1 lines 40-50; col. 13 lines 3-36); and

a pending insert state to a hidden state transition (col. 1 lines 40-50;col. 15 lines 10-25,col. 13 lines 3-36).

12. As per claim 9, Gostanian teaches a method the second set of element state transitions further comprises:

a pending insert state to a valid state transition(col. 15 lines 10-25);

a pending delete state to an invalid state transition(col. 15 lines 10-25,col. 13 lines 3-36).;

a hidden state to an invalid state transition(col. 13 lines 3-36);

a pending delete state to a valid state transition; a hidden state to a pending insert state transition and a pending insert state to an invalid state transition(col. 15 lines 10-25,col. 13 lines 3-36).

13. Claim 10 is rejected based on the same rejection as claim 1 above.

14. Claim 11 is rejected based on the same rejections as claim 1 above in addition Gostanian teaches queuing operation tasks in a task queue (col. 19 lines 5-40); and

receiving the queued operation tasks (col. 19 lines 5-40).

15. Claim 12 is rejected based on the same rejection as claim 11 above.

16. As per claim 13, Gostanian teaches a method inserting an element linked data structure comprising steps of:

performing a first set of operation tasks in a first phase, the first set of operation tasks operable to effect first set of element state transitions including a pre-associated state a pending insert state transition(col. 6 lines 6-17;col. 10 lines 30-50);

developing a second set operation tasks, the second set operation tasks operable to effect a second set element a pending insert state to a valid state transition(col. 15 lines 10-25,col. 13 lines 3-36); and

performing the second set of operation tasks in a second phase(col. 13 lines 40-65; col. 16 lines 53-57).

17. As per claim 14, Gostanian teaches a method wherein the pre-associated state to pending insert state transition is accomplished by:

marking the element to be inserted as being pre-associated to the data structure(col. 19 lines 16-21);

navigating the data structure to an insertion point(col. 1 lines 40-50);

creating links between the element to the be inserted and the data structure at the insertion point, the links created being visible only to the insertion operation; and

marking the element as being pending insert (col. 1 lines 40-50;col. 15 lines 10-25,col. 13 lines 3-36).

18. As per claim 15, Gostanian teaches a method wherein pending insert state a valid state transition accomplished by:

creating instructions for making created links visible to all operations(col. 1 lines 40-50; col. 19 lines 16-21); and

creating instructions for making existing links at the insertion point invisible to operations (col. 1 lines 40-50;col. 15 lines 10-25,col. 13 lines 3-36).

19. As per claim 16, Gostanian teaches a method wherein the step of performing the second set of operation tasks further comprises executing the created instructions including marking the element as valid (col. 14 lines 64-67;col. 19 lines 31-40; col. 14 lines 18-41).

20. Claims 17-20 are rejected based on the same rejections as claims 13-16 above.

21. Claim 21 is rejected based on the same rejection as claim10 above.

22. Claim 22 is rejected base don the same rejection as claim 13 above.

23. As per claim 23, Gostanian teaches a method for executing an operation upon a linked data structure having least one element, the method comprising steps of: dividing the operation into first and second distinct sets operation tasks(col. 13 lines 40-65; col. 16 lines 53-57);

performing the first set operation tasks first phase(col. 11 lines 12-40); and second set of operation tasks in performing the second phase(col. 13 lines 40-46).

24. As per claim 24, Gostanian teaches a method wherein the first set of operation tasks operable to maintain the linked data structure existing linked state(col. 14 lines 64-67;col. 19 lines 31-40; col. 14 lines 18-41).

25. As per claim 25, Gostanian teaches a method wherein the second set of operation tasks operable to modify existing linked state (col. 1 lines 40-50;col. 15 lines 10-25;col. 13 lines 3-36).

26. As per claim 26, Gostanian teaches a method wherein first of operation tasks is visible only to the operation (col. 1 lines 40-50;col. 15 lines 10-25; col. 13 lines 40-65; col. 16 lines 53-57).

27. As per claim 27, Gostanian teaches a method wherein the second set of operation tasks is visible to each plurality of operations upon the linked data structure(col. 13 lines 40-46).

28. As per claim 28, Gostanian teaches a system for executing an operation upon linked data structure having least one element, the system comprising:
memory for storing the linked data structure(col. 8 lines 25-50);
processor coupled memory, the processor operable to perform first set of operation tasks in first phase, first set of element state operable effect a first set of element state transitions to develop a second set of operation tasks, the second set of operation tasks operable effect second set element state transitions being distinct from the first set element state transitions; to perform the second set of operation tasks in a second phase(col. 1 lines 40-50;col. 15 lines 10-25; col. 13 lines 40-65; col. 16 lines 53-57).

29. Claim 29 is rejected based on the same rejection as claim 28 above.

30. Claim 30 is rejected based on the same rejections as claim 1 above.

31. Claim 31 is rejected based on the same rejection as claim 13 above.

32. Claim 32 is rejected based on the same rejections as claim 1 above.

33. Claim 33 is rejected based on the same rejection as claim 13 above.

34. Claim 34 is rejected based on the same rejection as claims 13 and 22 above.

35. Claim 35 is rejected based on the same rejection as claim 2 above.

36. Claim 36 is rejected based on the same rejection as claims 1 and 22 above.

37. Claims 37 -39 are rejected based on the same rejection as claim 14-16 above.

38. Claim 40 is rejected based on the same rejection as claim 16 above.

Conclusion

39. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nilesh Shah whose telephone number is (571)272-3771. The examiner can normally be reached on 9-5.Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100

40. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng An can be reached on (571)272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

41. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nilesh Shah
Examiner
Art Unit 2195

NS

April 28, 2005

MAJID BANANKHAH
PRIMARY EXAMINER